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Reduced Graphene Oxide Electrodes for Large Area Organic Electronics

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Devices based on solution processable organic materials are promising for inexpensive large area electronics on transparent flexible plastic substrates.[1] In practice, however, electrodes in organic devices typically consist of vacuum deposited materials that are largely incompatible with this goal. The most widely used transparent electrode for plastic electronics to date is tin-doped indium oxide (ITO). The latter provides a relatively high electrical conductivity ($\approx 10^4$ S cm^{-1})[6] with good optical transparency (>80%) for visible light.[7] Furthermore ITO has been used widely on plastic substrates, being compatible with high-throughput deposition processes such as sputtering. However, there are problems associated with ITO: i) it is brittle, which leads to micro-cracking when it is flexed and a consequent drop in conductivity, ii) there are concerns over the increasing cost of indium (rising from $\approx$350 to $\approx$1000 US$ per kg in recent years)[8] and its limited abundance, and iii) it is primarily suited to use as an anode material only because of its high work function. Hence there is a clear need for alternative materials, which rival or exceed the performance of ITO and other more traditional electrode metals.[9,10]

Graphene, an isolated single layer of graphite, has received much attention in recent years as a promising transparent electrode material.[11–13] The key challenges associated with its incorporation into practical electronic devices are finding scalable preparative routes and effective methods for laying down uniform films of graphene, ideally by existing proven deposition techniques. One promising method for preparing graphene is by chemical exfoliation of graphite oxide into graphene oxide sheets that can then be (partially) reduced to graphene by chemical and/or thermal treatments.[14–17] Significant progress has been made recently in the wafer-scale deposition of chemically

derived graphene (CDG) resulting in proof-of-concept demonstrations of its use as electrodes in various electronic devices such as photovoltaic,[18–20] light-emitting diodes,[21,22] and organic transistors[23] employing a variety of deposition techniques.[12,24,25] To address the specific challenge of integrating CDG-based electrodes into wafer-scale circuits, however, compatible patterning techniques must also be developed.

Here we demonstrate the patterning of CDG electrodes for use in organic field-effect transistors using the interlayer lithography method. This technique has previously been presented by Huang et al.[2,27,28] and Leem et al.[3,29] for the micrometer-scale patterning of molecular electrode materials and carbon nanotubes. The interlayer technique involves the insertion of a layer of photoresist between the substrate and the film to be patterned. The resist layer is exposed through a mask, generating a pattern that can subsequently be developed after deposition of the target material. Immersion in an appropriate developer removes the soluble parts of the resist layer together with the overlying target material, leaving a patterned film of the target material over a likewise patterned film of the resist. The resist and the target material are in effect patterned simultaneously in an expose–deposit–develop step sequence. Furthermore, this technique is compatible with the use of standard solution processing and mechanical transfer methods for deposition of the target films. Since interlayer lithography builds on the existing expertise and equipment of conventional photolithography, it is easy to implement and fully compatible with fast, cost effective sheet-to-sheet processing for large-area electronics.

The electrode fabrication process is schematically depicted in **Figure 1**. A detailed description of the CDG layer preparation is reported in the Experimental Section and elsewhere.[25] Briefly, a suspension of partially oxidized graphene in *N,N*-dimethylformamide (DMF) was synthesized by mild oxidation and intercalation of graphite. After purification by repeated centrifugation, a monolayer of partially oxidized graphene was formed by Langmuir–Blodgett assembly on a water surface. Several monolayers of the CDG were transferred (by repeated dipping) onto a glass substrate (Figure 1, step 1) and then annealed at 500 °C for one hour (step 2) to induce thermal reduction. Langmuir–Blodgett assembly allows layer-by-layer deposition of CDG where each deposition yields one monolayer film with a thickness of approximately 1 nm. After reduction, the CDG film was then coated with a poly(methyl methacrylate) (PMMA) backing layer and released from the glass substrate (step 3) and the PMMA-backed-CDG was transferred (CDG face down) (step 6) onto a pre-exposed SU8-2 photoresist layer on a glass substrate (steps 4–6). (Note, although glass is used for the work reported here, the interlayer patterning method has previously been applied to a wide range

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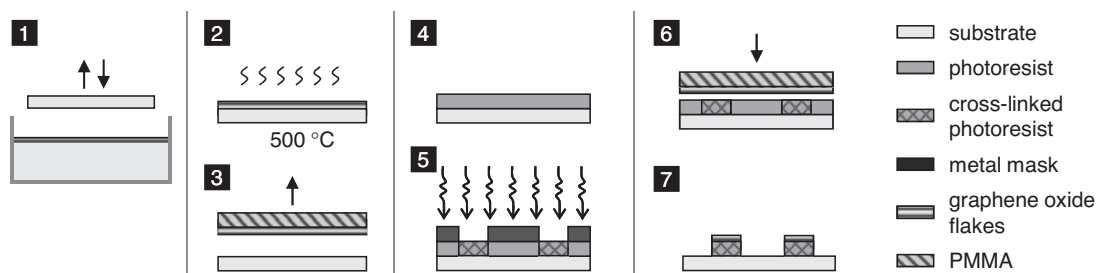
Figure 1. Interlayer lithography patterning of CDG electrodes. A thin film (4 nm) of CDG flakes is formed on a glass substrate by a Langmuir–Blodgett dip-coating technique (1). The CDG is partially reduced by annealing (2). Transfer of the conductive ultra-thin CDG layer by lamination onto exposed (4–5) SU8-2 photoresist with the help of a thin poly(methyl methacrylate) (PMMA) backing layer (3,6). Immersion in developer removes PMMA and un-crosslinked photoresist, resulting in patterned CDG electrodes with underlying crosslinked SU8-2 interlayer photoresist (7).

of other substrate materials including silicon, FR8 circuit board, and poly(ethylene terephthalate).) The entire substrate was then immersed in SU-8 developer and exposed to mild ultrasonication to yield the desired electrode pattern (step 7). A 4-layer CDG film, of approximately 4 nm thickness, exhibited transparency of ≈95% in the visible spectrum (**Figure 2**e) and had a sheet resistance of ≈30 kΩ per square. In comparison, much thicker (tens of nm) ITO films with a transparency of ≈90% typically exhibit sheet resistance of in the order of 0.01–0.1 kΩ per square.[30] We note, however, that recent work by Kim et al. has shown that large-area graphene films prepared on thin nickel foils by chemical vapor deposition and subsequently transferred by an equivalent process onto quartz can exhibit low sheet resistances of 280 Ω per square with 80% optical transmission.[31] The patterned CDG source and drain electrodes shown in the optical microscopy images of Figures 2a,b are separated by a channel length of 10 μm. Here, a conventional metal shadow mask was used to expose the SU8-2 interlayer photoresist. With optimized photolithography masks, high resolution patterns down to the

sub-micrometer regime can be routinely achieved[32] and have been previously demonstrated for interlayer lithography patterning of carbon nanotubess.[29] Figures 2c and d show the morphology of the CDG electrode edges and the underlying SU8-2 interlayer photoresist. No correlation between SU8-2 layer thickness and CDG electrode edge roughness could be observed. A possible explanation could be the ultra thin nature of the CDG electrodes as compared to the polymer layers.

The combination of solid-state transfer and interlayer patterning is very versatile and was employed here for both top-gate (TG) and bottom-gate (BG) transistor architectures. TG transistors were fabricated by sequential spin coating of an organic semiconductor and a fluorinated polymer gate dielectric (CYTOP) onto the as-patterned CDG source–drain electrodes (**Figure 3**a). The patterning and deposition from solution of the latter two components is less demanding and could alternatively be achieved with a variety of printing or stamping techniques, since micrometer-scale resolution/registration is not required. Here we employed i) a solution processable methanofullerene ([6,6]-phenyl-C_{61}-butyric acid ester ([60]PCBM)) and ii) a binary blend comprising a small molecule (8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT)) and a conjugated polymer (poly(triarylamine) (PTAA)) binder as two organic semiconductor exemplars.

The devices with [60]PCBM demonstrate the extraordinary suitability of CDG as a universal electrode material that is capable of injecting both holes and electrons into the semiconductor layer as evident from the ambipolar transistor characteristics shown in Figure 3b. The work function of CDG is approximately 4.5 eV and the frontier orbitals of [60]PCBM are located at 6.1 and 3.7 eV. Hence, the barriers for charge injection from CDG into [60]PCBM are large at approximately 1.6 eV for holes and 0.8 eV for electrons. Despite these significant barriers, especially for hole injection, the transistor exhibits ambipolar transport characteristics and can be operated either in the hole or electron accumulation regime depending on the biasing conditions (Figure 3b). Hole and electron mobilities derived where in the order of 10^{-3} and 10^{-2} cm² V⁻¹ s⁻¹, respectively. This
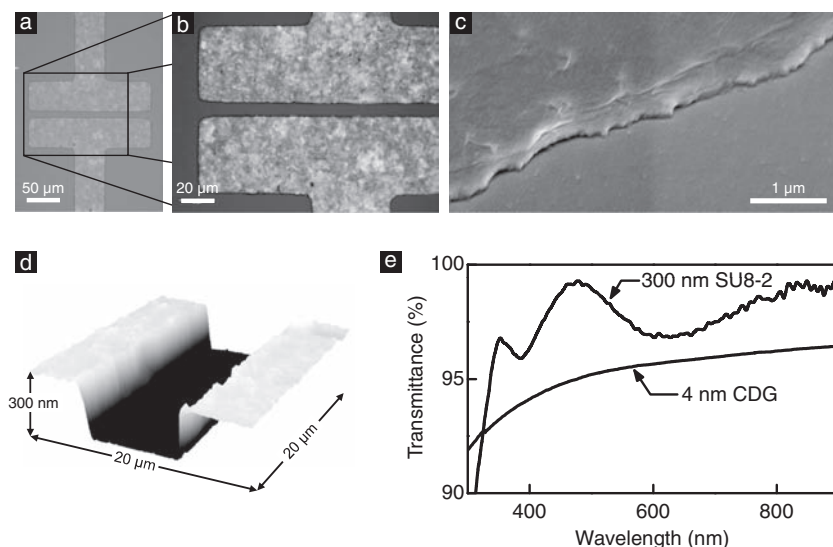
Figure 2. Patterned CDG source and drain electrodes for thin-film transistors. a,b) Optical microscopy images of patterned CDG electrodes with a 10 μm channel length. c) Scanning electron microscopy image of the patterned electrode edge, taken at an angle of ≈30°. d) Atomic force microscopy image illustrating the profile of the elevated source and drain electrodes. e) Transmittance graph of a 4 nm CDG film and a 300 nm SU8-2 film on quartz.

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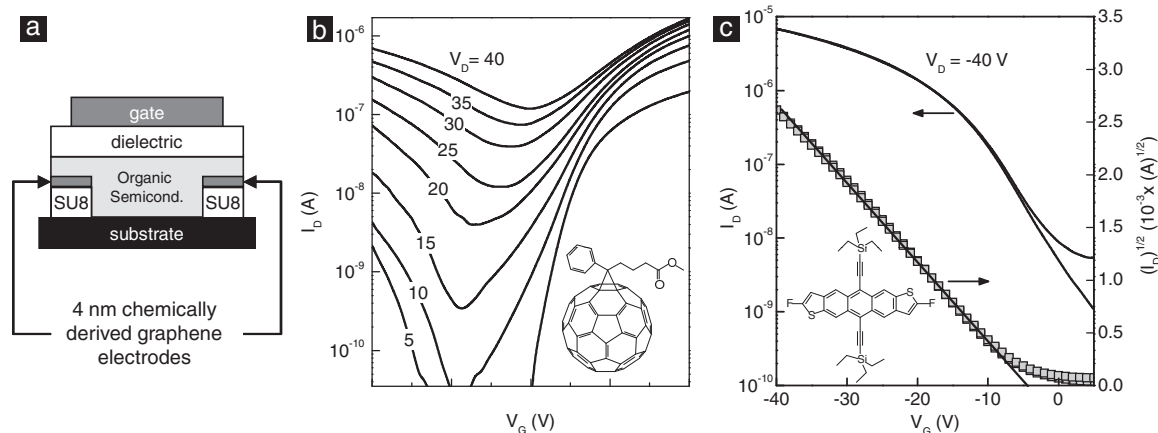
Figure 3. Organic field-effect transistors employing CDG source–drain electrodes. a) Schematic representation of TG transistor architecture. Transfer (drain current vs gate voltage) characteristics of b) ambipolar [60]PCBM (channel dimensions $L = 10\ \mu m$, $W = 200\ \mu m$) and c) p-type diF-TESADT:PTAA ($L = 40\ \mu m$, $W = 1000\ \mu m$) transistors. The molecular structures of the semiconductors are shown as insets.

quality of CDG makes complex fabrication steps, often required for the patterning of different electrode materials, i.e., a high and a low work function one, in organic complementary logic, redundant. It also enables facile fabrication of complementary-like logic using ambipolar semiconductors such as [60]PCBM. CDG thus proves to be a very versatile electrode material that is air-stable and can be processed in ambient conditions without any special precautions.

DiF-TESADT has been shown to be amongst the most promising solution-processable p-type organic semiconductors currently available.[24,33,34] Without further optimization of the blend composition and the electrode–semiconductor interface, hole mobilities of the order of 0.3 cm^2 V^{-1} s^{-1} were achieved in TG transistors (Figure 3c). This performance is remarkable, given the simple solution processing and film transfer/patterning methods employed to prepare the CDG electrodes.

Moving towards the integration of individual devices into circuit architectures, we also demonstrate a complementary inverter (**Figure 4**), utilizing an ambipolar and a p-channel transistor. The circuit employs CDG as a single, universal injecting electrode material, deposited as before in the solution phase and patterned by interlayer lithography. The operational characteristics of the complementary inverter in the first and third quadrant with a gain of ≈8 are displayed in Figure 4b. In principle, larger, more complex circuits employing CDG as the material of choice for electrodes and interconnects could be patterned using the interlayer lithography method. Compared to conventional microelectronics based on gold as the conducting material, the approach presented here provides optical transparency, enables facile solution processing, and paves the way towards high-performance, large-area microelectronics.

Finally, we demonstrate the compatibility of interlayer patterned graphene electrodes with novel, transistor architectures. One major handicap of state-of-the-art organic electronic devices has been the large operating voltages (>20 V) and high power consumption, which prevent their utilization in portable electronic devices. This problem can be alleviated by introducing ultra-thin (≈2.1 nm) high capacitance gate dielectrics, such as

self-assembled monolayer dielectrics.[4,5] Here a phosphono-hexadecanoic acid (**Figure 5**a) based self-assembled monolayer was functionalized on oxidized aluminium BG electrodes, followed by the interlayer lithographic patterning of the CDG source–drain electrodes. Remarkably, the patterning process is
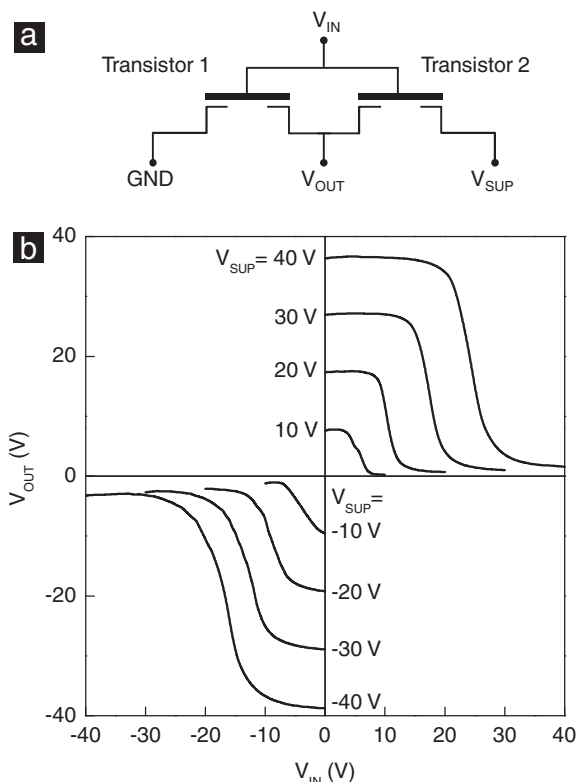
Figure 4. Complementary inverter circuit with conducting CDG electrodes. a) Circuit diagram of the complementary inverter employing an ambipolar [60]PCBM transistor ($L = 30\ \mu m$, $W = 500\ \mu m$) and a p-channel diF-TESADT:PTAA transistor ($L = 40\ \mu m$, $W = 1000\ \mu m$). b) Output characteristics of an inverter operating in the first and the third quadrant with a maximum gain of ≈8.
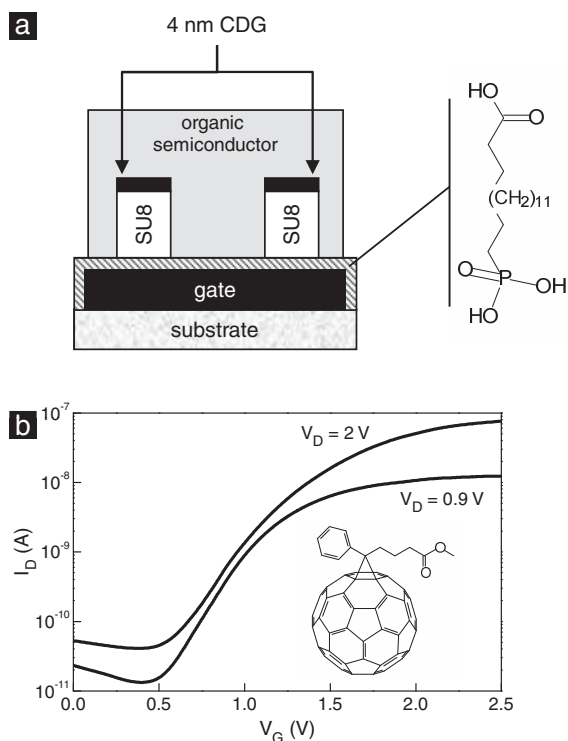
Figure 5. Low operating voltage BG transistors. a) Schematic of the BG architecture employing a self-assembled monolayer gate dielectric. b) Transfer characteristics of a low-voltage [60]PCBM transistor employing patterned CDG source–drain electrodes. Chemical structures of [60]PCBM and the self-assembled monolayer dielectric are also shown.

sufficiently gentle as to preserve the monolayer gate dielectric beneath and allow fabrication of the novel transistor architecture shown in Figure 5a. Using this structure in combination with [60]PCBM as the organic semiconductor, an n-channel transistor with electron mobility of $\approx 10^{-2}$ cm^2 V^{-1} s^{-1} and operation at voltages below 2.5 V has been achieved (Figure 5b). We note that this is the first demonstration of low-voltage operation for an organic transistor with CDG electrodes, an important requirement for practical application. We also emphasize that the dielectric, semiconductor, and source–drain electrodes are deposited from solution and all processes involved are compatible with easily scalable, large area deposition[25] and patterning methodologies.

Another interesting characteristic of our BG device architecture incorporating the SU8-2 photoresist interlayer beneath the source–drain electrodes is the reduced parasitic capacitance compared to conventional self-assembled monolayer-based BG devices.[4,5] The capacitances of the photoresist interlayer and the monolayer gate dielectric amount to ≈ 12 and ≈ 600 nF cm^{-2}, respectively, giving rise to a total parasitic capacitance between the source/drain electrodes and the gate of $C_{TOT} \approx 11.8$ nF cm^{-2}. In a typical analogue bottom contact device the parasitic capacitance would equal that of the gate dielectric, i.e., $C_{TOT} \approx 600$ nF cm^{-2}. This drastically reduced parasitic capacitance is expected to yield transistors with faster operating speeds, as compared to conventional self-assembled monolayer based organic field-effect transistors with similar overlaps,[5] and presents an

additional incentive for interlayer lithographic patterning.[35] However, further work would be required in order to establish the significance of this alternative transistor architecture.

In summary, we have demonstrated a methodology that exploits the outstanding qualities of chemically derived graphene for use as a transparent electrode material in large-area organic electronic applications. With the help of a simplified and versatile photolithographic technique known as interlayer lithography, highly conductive ultra-thin solution processed CDG films were patterned into source and drain electrodes with gaps down to 10 μm. Besides providing a suitable alternative to gold and transparent ITO electrodes, these patterned CDG electrodes allow for the fabrication of high performance field-effect transistors and complementary circuits that offer a viable route towards transparent organic electronics, fabricated entirely by solution processing.

Experimental Section

Deposition and Transfer of Chemically Derived Graphene: Partially oxidized graphene was synthesized by exfoliation of mildly oxidized graphite. Graphite (Sigma–Aldrich) was treated in a mixture of nitric acid and potassium chlorate for one week and washed with a copious amount of water. The product was intercalated by tetrabutylammonium hydroxide (TBA) in DMF and exfoliated into individual sheets. The resulting suspension was centrifuged repeatedly to remove unexfoliated particles and TBA. The purified suspension was spread on a water surface dropwise until a continuous monolayer of partially oxidized graphene sheets was formed. The monolayer was deposited onto a glass substrate by contact transfer (dip-coating). The deposition was repeated four times to form a 4-layer film. Reduction of partially oxidized graphene was achieved by annealing at 500 °C in a forming gas for 1 h. The reduced film was coated with a PMMA backing layer, separated from its original substrate, and then transferred (CDG face down) with the backing layer still attached onto a pre-exposed SU 8 photoresist layer on a glass substrate.[25]

Interlayer Lithography: SU8-2 photoresist (Microchem) was diluted with SU 8 thinner in a 1:3 weight ratio and spin-coated onto clean glass at 4000 rpm for 40 s. The resist was soft-baked on a hot plate at 65 °C for 1 min and at 95 °C for 1 min, before being exposed to 250 mJ cm^{-2} of 365 nm radiation using a Karl Suss MJB 3 mask aligner. After exposure, the resist was baked on a hot plate at 65 °C for 1 min and at 95 °C for 2 min. The CDG film (backed with PMMA) was laminated on top of the UV-exposed resist layer followed by annealing at 100 °C for 3 min. The CDG-coated resist layers were then developed using propylene glycol monomethyl ether acetate with the aid of mild sonication for 1 min, leaving a patterned layer of CDG on top of an identically patterned resist layer.

Transistor Fabrication and Characterization: For TG transistor architectures chlorobenzene solutions of [6,6]-phenyl-C$_{61}$-butyric acid ester ([60]PCBM) (20 mg mL^{-1}) or tetralin solutions of a 50:50 wt% blend of 8-difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TESADT) with poly(triarylamine) (PTAA) were spin coated onto the interlayer lithography patterned CDG source–drain electrodes in a nitrogen atmosphere. As gate dielectric the fluoropolymer CYTOP (Asahi Glass Co.) was spin coated at 2000 rpm and dried at 90 °C for 15 min. An aluminium TG electrode was evaporated through a shadow mask. For the low operating voltage BG transistors, aluminium gate electrodes were evaporated through a shadow mask on to glass and their surface was oxidized by brief exposure to a low power, oxygen plasma. Phosphonohexadecanoic acid in isopropyl alcohol was drop cast onto and rinsed off the substrate (repeated several times to ensure full coverage), followed by baking at 140 °C for several hours. Patterning of the source–drain electrodes by interlayer lithography was then performed

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on these substrates, in alignment with the previously deposited gate electrodes. Finally, the semiconductor layer ([60]PCBM) was deposited by spin-coating in a nitrogen atmosphere. All measurements were performed at room temperature in nitrogen atmosphere using a Keithley SCS4200 Semiconductor Parameter Analyzer.

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